IN THE CLAIMS:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising a first conductive layer and a second conductive layer;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern with the tapered sidewall portion; and

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching.

2. (Previously Presented) The method according to claim 1, wherein the plasma treatment is an argon plasma treatment.

3. (Previously Presented) The method according to claim 1, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

4. (Previously Presented) The method according to claim 1, wherein the first conductive layer is made of a metal nitride.

5. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising first conductive layer and a second conductive layer including titanium as its main component;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern with the tapered sidewall portion; and

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching.

6. (Previously Presented) The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

7. (Previously Presented) The method according to claim 5, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

8. (Previously Presented) The method according to claim 5, wherein the first conductive layer is made of metal nitride.

9. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer, and a third conductive layer on the second conductive layer;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern with the tapered sidewall portion; and

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching.

10. (Previously Presented) The method according to claim 5, wherein the plasma treatment is an argon plasma treatment.

11. (Previously Presented) The method according to claim 5, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

12. (Previously Presented) The method according to claim 5, wherein the first conductive layer is made of a metal nitride.

13. (Previously Presented) The method according to claim 5, wherein the third conductive layer is made of a metal having high-melting point.

14. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer including titanium as its main

component on the first conductive layer, and a third conductive layer on the second conductive layer;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern; with the tapered sidewall portion; and

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching.

15. (Previously Presented) The method according to claim 14, wherein the plasma treatment is an argon plasma treatment.

16. (Previously Presented) The method according to claim 14, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

17. (Previously Presented) The method according to claim 14, wherein the first conductive layer is made of a metal nitride.

18. (Previously Presented) The method according to claim 14, wherein the third conductive layer is made of a metal having high-melting point.

19. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising a first conductive layer and a second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern with the tapered sidewall portion;

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching; and

adding an impurity elements to the semiconductor layer with the second conductive layer as a shielding mask to form a region with the impurity elements in the semiconductor film,

wherein the region with the impurity elements overlaps with the first conductive layer.

20. (Previously Presented) The method according to claim 19, wherein the plasma treatment is an argon plasma treatment.

21. (Previously Presented) The method according to claim 19, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

22. (Previously Presented) The method according to claim 19, wherein the first conductive layer is made of a metal nitride.

23. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern on a laminate comprising a first conductive layer, a second conductive layer on the first conductive layer, and a third conductive layer on the second conductive layer over a semiconductor layer with a gate insulating film interposed therebetween;

forming a first pattern with a tapered sidewall portion by etching the laminate;

performing a plasma treatment to the first pattern with the tapered sidewall portion;

forming a second pattern by ~~anisotropic etching~~ removing the tapered sidewall portion of the first pattern with ~~the tapered sidewall portion~~ anisotropic etching; and

adding an impurity elements to the semiconductor layer with the second conductive layer and the third conductive layer as a shielding mask to form a region with the impurity elements in the semiconductor film,

wherein the region with the impurity elements overlaps with the first conductive layer.

24. (Previously Presented) The method according to claim 23, wherein the plasma treatment is an argon plasma treatment.

25. (Previously Presented) The method according to claim 23, wherein a reaction product adhering to the tapered sidewall portion is removed by the performing the plasma treatment step.

26. (Previously Presented) The method according to claim 23, wherein the first conductive layer is made of a metal nitride.

27. (Previously Presented) The method according to claim 23, wherein the third conductive layer is made of a metal having high-melting point.

28-32. (Canceled)